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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,055	08/26/2003	Tapan J. Chakraborty	CHAKRABORTY 8-2	2959

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EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,055	CHAKRABORTY ET AL.	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Chakraborty et al. (IEEE Paper 'A Novel Fault Injection Method for System Verification Based on FPGA Boundary Scan Architecture').

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

3. As per claim 1, Chakraborty et al. discloses a fault selection circuit adapted with fault selection data identifying selected circuit outputs of the circuit device, a fault value circuit adapted with fault values for injection on corresponding selected circuit outputs, and the fault selection circuit controlling the selected circuit outputs in place of control by system logic during injection of respective fault values on pages 925-926, under

heading '3 Proposed Fault Injection Method', number 3 - "To avoid the rippling effect...the fault injection data".

4. As per claim 2, Chakraborty et al. discloses the data and the fault values, respectively, are received from an industry standard, TAP controller on page 926, number 3 – "The control signal...to store the fault injection data".

5. As per claim 3, Chakraborty et al. discloses wherein, the circuit device comprises a field programmable gate array, FPGA on page 923, the abstract.

6. As per claim 4, Chakraborty et al. discloses wherein, the circuits are independent of an operating system of the circuit device on page 926, under the heading '4 Experimental Results', "To implement our proposed fault injection method...the LEDs of the board." and on page 927, "Example 1...fault injection." There is no disclosed operating system on the demo board.

7. As per claim 5, Chakraborty et al. discloses wherein, the system selects pins for fault injection, and the pins are connected to a circuit board having circuit board interconnections being tested for vector verification by the fault injection values on page 927, "The fault injection software tool...verify if fault are properly injected." and on page 927, "Example 1...We applied interconnect test vectors...for fault injection."

8. As per claim 6, Chakraborty et al. discloses wherein, the system selects pins for fault injection, the pins are connected to a backplane, and the backplane is coupled to a backplane test tool having a backplane test algorithm being tested for verification on page 927, "The fault injection software tool...verify if fault are properly injected." and on

page 928, "Example 2: Verification of a new backplane test algorithm...diagnosis capability."

9. As per claim 7, Chakraborty et al. discloses wherein, the fault selection circuit comprises a user defined scan register in the circuit device on pages 925-926, under heading '3 Proposed Fault Injection Method', number 3 - "To avoid the rippling effect...the fault injection data".

10. As per claim 8, Chakraborty et al. discloses the fault value circuit comprises a user defined scan register in the circuit device on pages 925-926, under heading '3 Proposed Fault Injection Method', number 3 - "To avoid the rippling effect...the fault injection data".

11. As per claim 9, Chakraborty et al. discloses the system selects an internal register for fault injection, and the internal register is in the system logic of the circuit device on page 928, under heading '5 Conclusion', "The resulting BS architecture is still compliant... via BS while the system is online."

12. As per claim 10, Chakraborty et al. discloses storing and updating fault injection selection data in a first register; scanning and storing fault injection values in a second register; and updating the fault injection selection data and the fault injection values at the selected fault injection locations of the programmable circuit device, while the selected fault injection locations are controlled by the first and second register instead of by system logic of the circuit device on pages 925-926, under heading '3 Proposed Fault Injection Method', number 3 - "To avoid the rippling effect...the fault injection data".

13. As per claim 11, Chakraborty et al. discloses injecting stuck-on fault injection values on selected pins of the fault injection locations on page 927, "The fault injection software tool...verify if fault are properly injected." Examiner interprets by way of the specification that the stuck-on is the stuck-open.

14. As per claim 12, Chakraborty et al. discloses injecting stuck-at fault injection values on selected pins of the fault injection locations on page 927, "The fault injection software tool...verify if fault are properly injected."

15. As per claim 13, Chakraborty et al. discloses injecting stuck-on fault injection values on selected pins of the fault injection locations; and injecting stuck-at fault injection values on selected pins of the fault injection locations on page 927, "The fault injection software tool...verify if fault are properly injected."

16. As per claim 14, Chakraborty et al. discloses injecting stuck-on fault injection values on selected pins of the fault injection locations while the programmable circuit device is mounted on a circuit board, to test for vector verification of circuitry of the circuit board on page 927, "The fault injection software tool...verify if fault are properly injected." and on page 927, "Example 1...We applied interconnect test vectors...for fault injection."

17. As per claim 15, Chakraborty et al. discloses injecting stuck-at fault injection values on selected pins of the fault injection locations while the programmable circuit device is mounted on a circuit board, to test for vector verification of circuitry of the circuit board on page 927, "The fault injection software tool...verify if fault are properly

injected." and on page 927, "Example 1...We applied interconnect test vectors...for fault injection."

18. As per claim 16, Chakraborty et al. discloses injecting stuck-on fault injection values on selected first pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the first pins, while the programmable circuit device is mounted on a circuit board, to test for vector routing verification of the circuit board; and injecting stuck-at fault injection values on selected second pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the second pins, while the programmable circuit device is mounted on a circuit board, to test for vector routing verification of the circuit board on page 927, "The fault injection software tool...verify if fault are properly injected." and on page 927, "Example 1...We applied interconnect test vectors...for fault injection."

19. As per claim 17, Chakraborty et al. discloses injecting stuck-on fault injection values on selected first pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the first pins, while the programmable circuit device is mounted on a circuit board being tested by verification test software, to test for verification of a new algorithm of the software; and. injecting stuck-at fault injection values on selected second pins of the fault injection locations connected in a fault injection circuit between system logic of the programmable circuit device and the second pins, while the programmable circuit device is mounted on a circuit board being tested by verification test software, to test for

verification of a new algorithm of the software on page 927, "The fault injection software tool...verify if fault are properly injected." and on page 928, "Example 2: Verification of a new backplane test algorithm...diagnosis capability."

20. As per claim 18, Chakraborty et al. discloses injecting one or more of the fault injection values at an internal register in the system logic of the circuit device on page 928, under heading '5 Conclusion', "The resulting BS architecture is still compliant... via BS while the system is online."

Claim Objections

21. Claim 11 is objected to because of the following informalities: In claim 11, 'further comprising;' should be 'further comprising:'. Appropriate correction is required.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Yolanda L Wilson
Examiner
Art Unit 2113